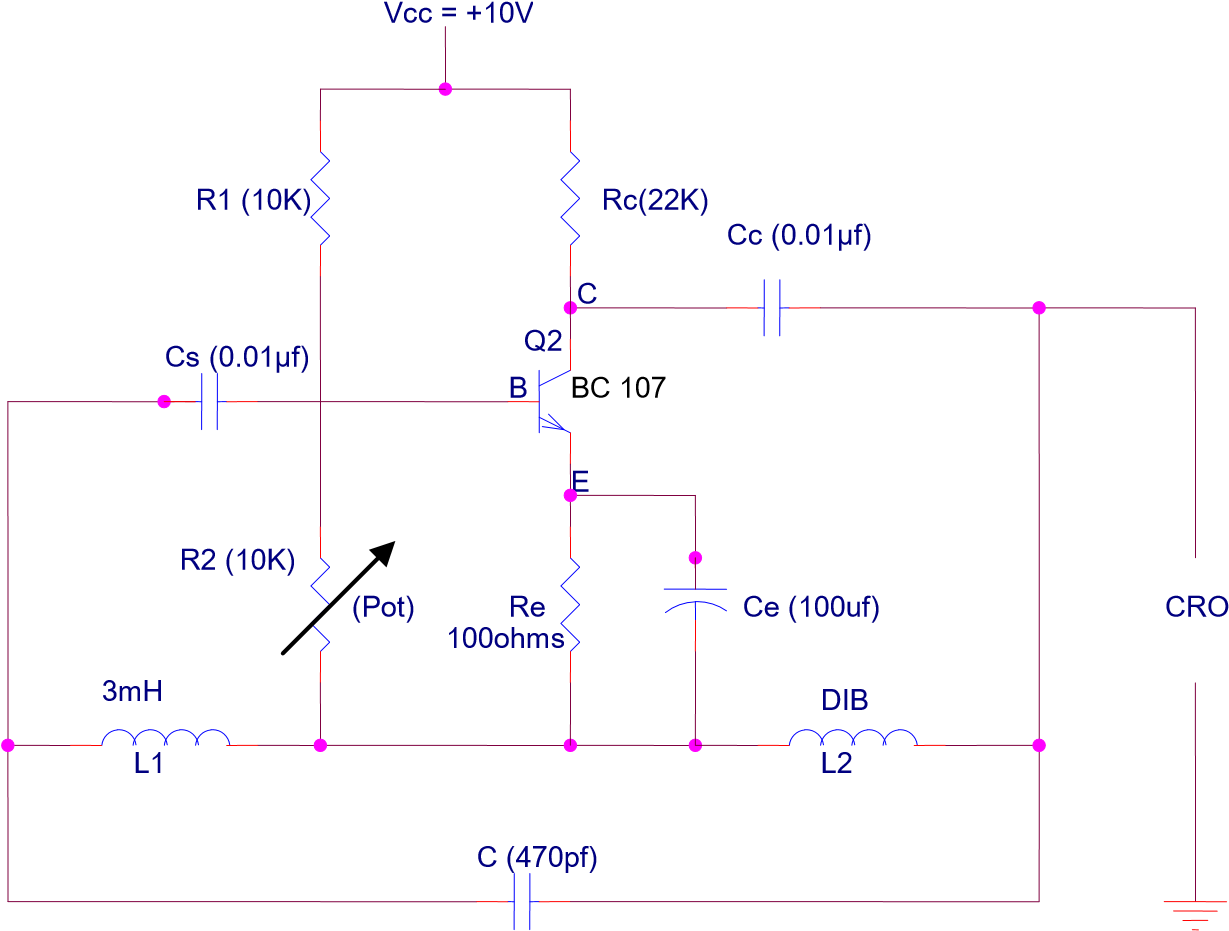
**7. HARTLEY OSCILLATOR**

**AIM:**  To determine the frequency of oscillations of Hartley oscillator.

**APPARATUS:**  1. BC 107 Transistor,

1. Potentiometer 10KΩ (1),
2. Resistors – 10KΩ (1), 22KΩ (1) & 100Ω (1),
3. Capacitors –10µf(2), 100µf(1) & 470pf(1),
4. Inductor 100µH (1),
5. Decade Inductance Box (2),
6. TRPS,
7. Bread Board and connecting wires,
8. CRO with probes

**CIRCUIT DIAGRAM** :



# HARTLEY OSCILLATOR

**PROCEDURE**:

1. Connections are made as shown in circuit diagram.
2. The inductor ‘L2’ is up to some value, keeping inductor ‘L1’ constant.
3. The potentiometer ‘R2’ is adjusted until sinusoidal waveform is observed on

CRO.

1. The time period and hence the frequency are calculated for the wave obtained which is nearly equal to the theoretical frequency.
2. The experiment is repeated for different values of ‘L2’ and each time the time period is noted.

**CALCULATION:**

1. L1 = 3mH and L2 = 3mH ,

C = 470pf

Leq = L1 + L2 = 6mH

theoretical frequency, f= 1 2𝜋√LeqC,

f= 94823.46 Hz

1. L1 = 3mH and L2 = 4mH ,

C = 470pf

Leq = L1 + L2 = 7mH

theoretical frequency, f= 1 2𝜋√LeqC,

f= 87789.465 Hz

1. L1 = 3mH and L2 = 5mH ,

C = 470pf

Leq = L1 + L2 = 8mH

theoretical frequency, f= 1 2𝜋√LeqC,

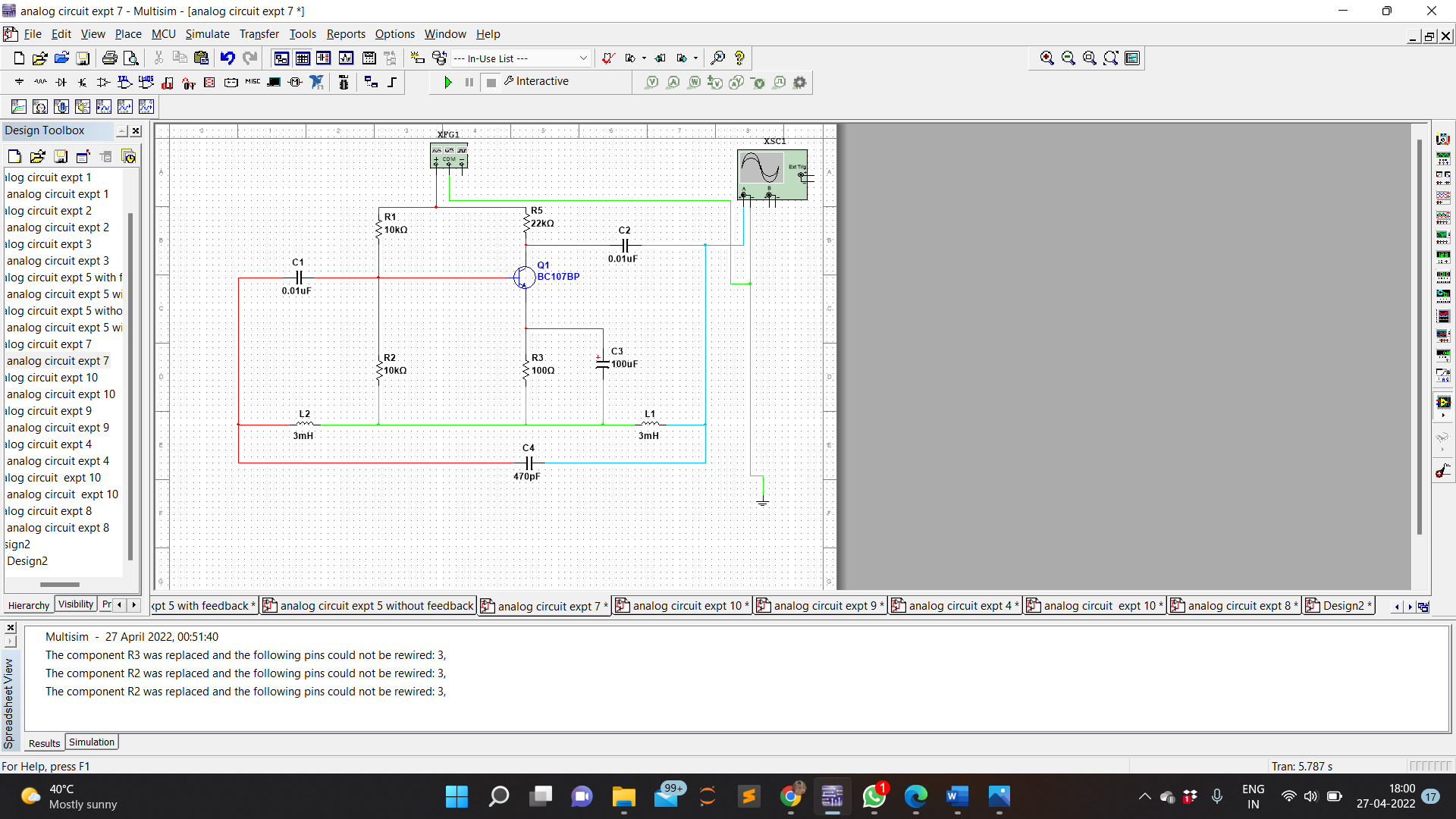
f= 82119.525 Hz

**TABULAR FORM:**

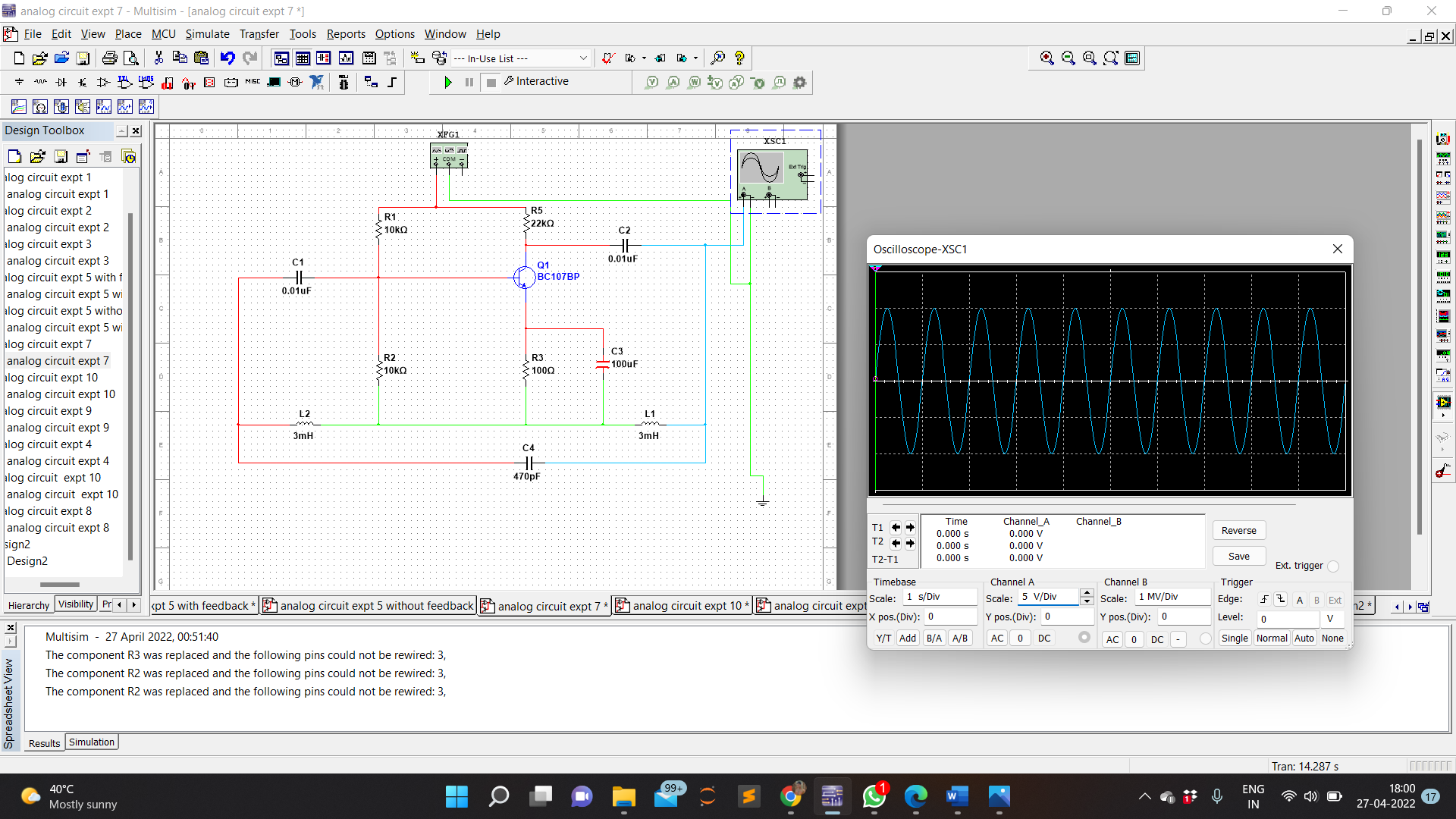
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **C** |  | **Inductance** | | **Theoretical f = 1 /2П√Leq C** | **Time**  **T (Sec)** |
| **L1** | **L2** | **Leq =L1+ L2** |
| **470pf**    **470pf**    **470pf** | **3mH**    **3mH**    **3mH** | **3mH**    **4mH**    **5mH** | **6mH**  **7mH**  **8mH** | **94823.46 Hz**  **87789.465 Hz**  82119.525 Hz | 0.0000105  0.0000113  0.0000121 |

**GRAPH:** A graph is plotted between time period on x-axis and Amplitude on y-axis to obtained a sinusoidal waveform at a particular value of L2.

CIRCUIT DIAGRAM



WAVEFORM



**PRECAUTIONS**: 1. Avoid loose contacts.

2. Avoid wrong connections.

**RESULT**: Frequency of oscillations of Hartley oscillator has been studied and calculated through the designed circuit.